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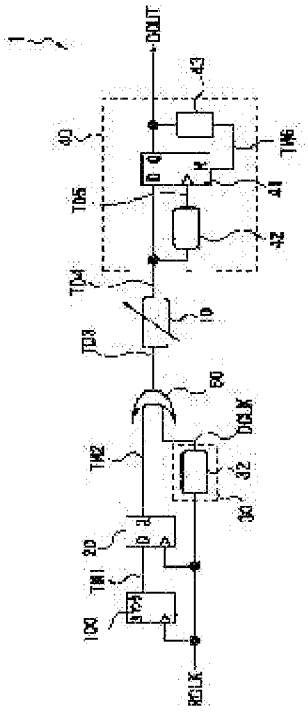
(54) DELAY TIME STABILIZING CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a delay time stabilizing circuit that does not deteriorate timing accuracy independently of frequency fluctuations of an input signal even when a CMOS circuit is employed for a minute timing generating circuit.

SOLUTION: The delay time stabilizing circuit 1 of this invention is provided with a dummy pulse generating means 30 and a pulse mixer means 50 that insert a dummy pulse signal whose pulse width differs from that of a target signal into between the target signal and a target signal desirably to be delayed in order to reduce fluctuations in the operating frequency of the circuit 1 and that are placed between a flip-flop 20 and a vernier 10 in a conventional circuit, and with a signal extract means 40 that discriminates the target signal from the dummy pulse signal depending on the difference in the pulse width, extracts only the target signal and is placed after the output of the vernier 10. Thus, the circuit 1 decreases the fluctuations in the operating frequency of the vernier 10 independently of the number of increased/decreased passing times of the target signal so as to reduce fluctuations in the power consumption of the vernier 10 thereby stabilizing the delay time.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the detailed timing generating circuit of an LSI tester, and relates to the time delay stabilization circuit at the time of constituting a circuit from CMOS in detail.
[0002]
[Description of the Prior Art]Conventionally, the timing generating circuit is constituted by ECL. Since ECL comprises a current regulator circuit, it is not based on the clock frequency of a circuit, but its power consumption is fixed.For this reason, it is not concerned with a wave-like passage interruption fault, but the temperature change of a circuit has the characteristic that it is few and few delay time variations of an input signal are. Hereafter, the detailed timing generating circuit of the LSI tester constituted by conventional ECL is explained based on drawing 6 and drawing 7.
[0003]Drawing 6 is a circuit diagram showing an example of the timing generating circuit constituted by conventional ECL. As shown in drawing 6, the timing generating circuit 6 comprises the counter 100, and the flip-flop 20 and the vernier 10 which are detailed timing generating circuits.
[0004]The counter 100 is outputted as signal TM1 which calculated the cycle for the time delay of the request set up beforehand, and delayed it from the count start signal which does not illustrate the inputted reference signal RCLK. The flip-flop 20 outputs signal TM1 inputted from the counter 100 as signal TM2 which carried out retiming with the reference signal RCLK. The vernier 10 is outputted as the signal TOUT with which only the delaying amount of the request beforehand set up with the resolution below the cycle T of the reference signal RCLK delayed signal TM2 inputted from the flip-flop 20.
[0005]Drawing 7 is a timing chart which shows the state of each signal in the timing generating

circuit 6 of drawing 6. A circuit's own signal delay is omitted for simplification.
[0006]The reference signal RCLK is a reference signal given to a circuit with the constant period T. Signal TM1 is the signal delayed from the count start signal over the counter 100 which is not illustrated by the integral multiple of the cycle T of the reference signal RCLK with the preset value of the counter. Since the preset value of a counter can be changed arbitrarily, the interval of a pulse and a pulse is not constant. Signal TM2 is the waveform which carried out retiming of signal TM1 with the reference signal RCLK with the flip-flop 20, and carried out 1 case shift. The signal TOUT is the waveform which delayed TM2 with the resolution below the cycle T of the reference signal RCLK by the vernier 10.
[0007]
[Problem(s) to be Solved by the Invention]However, if it is in such a conventional detailed timing generating circuit, Since the directions of CMOS are high integration, low power consumption, and low cost compared with ECL, in recent years, the demand which constitutes a circuit from CMOS is increasing also in the detailed timing generating circuit which needs high timing accuracy.
[0008]However, CMOS had the characteristic which is not preferred of degrading timing accuracy, to the demand of high timing accuracy, when the circuit was a state of rest, electric power was specifically consumed hardly, but there was a problem that power consumption will increase with the increase in the clock frequency of a circuit. For this reason, if the clock frequency of a circuit changes, a circuit's own calorific value will change, and the temperature of a circuit will change. And load driving capability changed by change of the temperature of a circuit, and there was a problem of changing a time delay.
[0009]Here, the detailed timing generating circuit constituted from conventional ECL of drawing 6 is transposed to CMOS, and is explained. In drawing 7, signal TM2 inputted into the vernier 10 does not have a constant pulse passing number per time. Then, with the characteristic of above-mentioned CMOS, since the power consumption of the vernier 10 does not become fixed, temperature is not stabilized but the situation where a actual delaying amount is not stabilized to the time delay set up as a result occurs.
[0010]Although the vernier 10 is a circuit which acquires a time delay with the variable resolution below a reference signal, since it has a time delay more than the cycle of a reference signal at least including the fixed delay of a vernier at the time of maximum delay setting out, compared with other logic gates, the delay time variations to a temperature change will become large.
[0011]Even if the technical problem of this invention creates a detailed timing generating circuit in a CMOS circuit, it is providing the time delay stabilization circuit which is not concerned with the frequency change of an input pulse signal, and does not degrade timing accuracy.
[0012]

[Means for Solving the Problem]The invention according to claim 1 equips with the following a time delay stabilization circuit which outputs a timing signal with delay resolution below a cycle of a reference signal of constant frequency.
An input pulse creating means which makes an inputted reference signal of constant frequency a clock pulse signal, and generates an input pulse signal to arbitrary times with resolution of a cycle of said reference signal by making one cycle of said reference signal into pulse width (for example, counter 100 shown in drawing 1).
1st pulse holding mechanism outputted while holding said input pulse signal by front edge of said reference signal (for example, flip-flop 20 shown in drawing 1).
A dummy pulse creating means (for example, dummy pulse generating circuit 30 shown in drawing 1) which generates a dummy pulse signal of different pulse width from a cycle of this reference signal based on said input pulse signal or said reference signal, The 1st logical sum means that carries out OR operation of the 1st maintenance pulse signal outputted from said 1st pulse holding mechanism, and the dummy pulse signal outputted from said dummy pulse creating means, and outputs a mixed pulse signal. The 1st pulse delay means that delays (for example, OR gate 50 shown in drawing 1), and time beforehand set up with delay resolution below a cycle of said reference signal in a mixed pulse signal outputted from said 1st logical sum means, and outputs the 1st delay pulse signal (for example). By the difference in pulse width of the vernier 10 shown in drawing 1, and said input pulse signal and a dummy pulse signal. A signal pulse extraction means to remove a dummy pulse signal from the 1st delay pulse signal outputted from said 1st pulse delay means, and to extract and output only a delay pulse signal of said input pulse signal (for example, signal pulse extracting circuit 40 shown in drawing 1).

[0013]According to this invention according to claim 1, in a time delay stabilization circuit to output, a timing signal with delay resolution below a cycle of a reference signal of constant frequency an input pulse creating means, Make an inputted reference signal of constant frequency into a clock pulse signal, generate a pulse signal inputted into arbitrary times with resolution of a cycle of a reference signal by making one cycle of a reference signal into pulse width, and by the 1st pulse holding mechanism. Output holding an input pulse signal by front edge of a reference signal, and a dummy pulse creating means, Based on an input pulse signal or a reference signal, generate a dummy pulse signal of different pulse width from a cycle of a reference signal, and the 1st logical sum means, Carry out OR operation of the 1st maintenance pulse signal outputted from the 1st pulse holding mechanism, and the dummy pulse signal outputted from a dummy pulse creating means, and a mixed pulse signal is outputted, The 1st pulse delay means delays time beforehand set up with delay resolution below a cycle of a reference signal in a mixed pulse signal outputted from the 1st logical sum

means, outputs the 1st delay pulse signal, and a signal pulse extraction means by the difference in pulse width of an input pulse signal and a dummy pulse signal. Since a dummy pulse signal is removed from the 1st delay pulse signal outputted from the 1st pulse delay means and only a delay pulse signal of an input pulse signal is extracted and outputted, it is not concerned with a change in an input pulse signal, but clock frequency change of the vernier 10 can be made small. Since power consumption change of the vernier 10 becomes small by this, a temperature change becomes small and, therefore, can stabilize a time delay.
[0014]In the invention according to claim 1, the invention according to claim 2 a dummy pulse creating means, From a time delay from an input of a clock pulse signal of said 1st pulse holding mechanism to an output of the 1st maintenance pulse signal, it is large and and within time of difference of a cycle of said reference signal, and pulse width of this reference signal, It has further the 2nd pulse delay means (for example, delay circuit 32 shown in drawing 1) that delays said reference signal, and generates and outputs a dummy pulse signal.
[0015]According to this invention according to claim 2, in the invention according to claim 1 a dummy pulse creating means, By the 2nd pulse delay means, from a time delay from an input of a clock pulse signal of the 1st pulse holding mechanism to an output of the 1st maintenance pulse signal, it is large and and within time of difference of a cycle of a reference signal, and pulse width of a reference signal, Since a reference signal is delayed and a dummy pulse signal is generated and outputted, a dummy pulse signal which delayed a reference signal with which pulse width differs can be inserted between an input pulse signal and an input pulse signal which you want to delay, and clock frequency change of a circuit can be made small.
[0016]In the invention according to claim 1 or 2, the invention according to claim 3 said signal pulse extraction means, It is larger than pulse width of a dummy pulse signal included in said 1st delay pulse signal outputted from said 1st pulse delay means, And within difference of a time delay of said dummy pulse generating circuit from an input of said reference signal to a dummy pulse signal output, and a cycle of said reference signal, The 3rd pulse delay means (for example, delay circuit 42 shown in drawing 1) that delays said 1st delay pulse signal and outputs the 3rd delay pulse signal,The 3rd delay pulse signal outputted from said 3rd pulse delay means is made into a clock pulse signal, Said 1st delay pulse signal is held by front edge of this clock pulse signal, The 2nd pulse holding mechanism (for example, flip-flop 41 shown in drawing 1) that removes a delay pulse signal of a dummy pulse signal included in said 1st delay pulse signal, and extracts a delay pulse signal of said input pulse signal, The 4th pulse delay means that delays said 2nd maintenance pulse signal and resets said 2nd pulse holding mechanism so that it may become the pulse width set up beforehand about the 2nd maintenance pulse signal outputted from said 2nd pulse holding mechanism (for example) It has further the delay circuit 43 shown in drawing 1. [0017]According to the invention according to claim 3, in the invention according to claim 1 or 2 a signal pulse extraction means, It is larger

than pulse width of a dummy pulse signal included in the 1st delay pulse signal outputted from the 1st pulse delay means by the 3rd pulse delay means, And within difference of a time delay of a dummy pulse generating circuit from an input of a reference signal to a dummy pulse signal output, and a cycle of a reference signal, Delay the 1st delay pulse signal, output the 3rd delay pulse signal, and by the 2nd pulse holding mechanism. The 3rd delay pulse signal outputted from the 3rd pulse delay means is made into a clock pulse signal, Hold the 1st delay pulse signal by front edge of a clock pulse signal, remove a delay pulse signal of a dummy pulse signal included in the 1st delay pulse signal, extract a delay pulse signal of an input pulse signal, and by the 4th pulse delay means. Since the 2nd maintenance pulse signal is delayed and the 2nd pulse holding mechanism is reset so that it may become the pulse width set up beforehand about the 2nd maintenance pulse signal outputted from the 2nd pulse holding mechanism, Since an input pulse signal and a dummy pulse signal are distinguished by the difference in pulse width and only a delay pulse signal of an input pulse signal can be extracted, The conventional timing generating circuit and a time delay stabilization circuit which performs same operation can be constituted.

[0018]According to the invention according to claim 4, in the invention according to claim 1 said dummy pulse creating means, The 1st maintenance pulse signal outputted from said 1st pulse holding mechanism, The 2nd logical sum means that carries out OR operation of the inversion signal of the 3rd maintenance pulse signal outputted from the 3rd pulse holding mechanism (for example, flip-flop 34 shown in drawing 3) mentioned later, and outputs the 1st mask signal. (For example, OR gate 33 shown in drawing 3) and said reference signal are made into a clock pulse signal, The 3rd [said] pulse holding mechanism holding the 1st mask signal outputted from said 2nd logical sum means by the front edge, An inversion signal of the 3rd maintenance pulse signal outputted from said 3rd pulse holding mechanism, The 1st AND means (for example, AND gate 301 shown in drawing 3) that carries out the AND operation of said input pulse signal, and outputs a toggle enable signal, A torr gouy navel orange signal outputted from said 1st AND means, and the 4th pulse holding mechanism mentioned later. An exclusive OR means (for example, EXOR gate 302 shown in drawing 3) which carries out EXCLUSIVE OR operation of the 4th maintenance pulse signal outputted from (for example, the flip-flop 303 shown in drawing 3), and outputs the 2nd mask signal, The 4th [said] pulse holding mechanism holding the 2nd mask signal outputted from said exclusive OR means by the front edge by making said reference signal into a clock pulse signal, An after [a logical product] logic inversion means (for example, NAND gate 304 shown in drawing 3) to do the after [a logical product] logic inversion operation of the 4th maintenance pulse signal and said input pulse signal outputted from said 4th pulse holding mechanism, and to output a reversal mask signal, It exceeds time adding a time delay of said 4th pulse holding mechanism, and a time delay of said after [a logical product] logic inversion means, And the 2nd pulse delay

means (for example, delay circuit 32' shown in drawing 3) that delays said reference signal within time of a cycle and difference of pulse width of said reference signal, and outputs the 2nd delay pulse, An inversion signal of the 3rd maintenance pulse signal outputted from said 3rd pulse holding mechanism, The 2nd AND means that does the theoretical product operation of a reversal mask signal outputted from said after [a logical product] logic inversion means, and the 2nd delay pulse signal outputted from said 2nd pulse delay means, and generates and outputs a dummy pulse signal. (For example, AND gate 35 shown in drawing 3) It has further.

[0019]According to the invention according to claim 4, in the invention according to claim 1 a dummy pulse creating means, The 1st maintenance pulse signal outputted from the 1st pulse holding mechanism by the 2nd logical sum means, Carry out OR operation of the inversion signal of the 3rd maintenance pulse signal outputted from the 3rd pulse holding mechanism mentioned later, output the 1st mask signal, and by the 3rd pulse holding mechanism. Hold the 1st mask signal outputted from the 2nd logical sum means by the front edge by making a reference signal into a clock pulse signal, and by the 1st AND means. Carry out the AND operation of an inversion signal of the 3rd maintenance pulse signal outputted from the 3rd pulse holding mechanism, and the input pulse signal, output a toggle enable signal, and by an exclusive OR means. Carry out EXCLUSIVE OR operation of a torr gouy navel orange signal outputted from the 1st AND means, and the 4th maintenance pulse signal outputted from the 4th pulse holding mechanism mentioned later, output the 2nd mask signal, and by the 4th pulse holding mechanism. Hold the 2nd mask signal outputted from an exclusive OR means by the front edge by making a reference signal into a clock pulse signal, and by an after [a logical product] logic inversion means. Carry out after [a logical product] logic inversion of the 4th maintenance pulse signal and input pulse signal that were outputted from the 4th pulse holding mechanism, output a reversal mask signal, and by the 2nd pulse delay means. It exceeds time adding a time delay of the 4th pulse holding mechanism, and a time delay of an after [a logical product] logic inversion means, And delay a reference signal within time of a cycle and difference of pulse width of a reference signal, output the 2nd delay pulse, and by the 2nd AND means. An inversion signal of the 3rd maintenance pulse signal outputted from the 3rd pulse holding mechanism, Since the AND operation of a reversal mask signal outputted from an after [a logical product] logic inversion means and the 2nd delay pulse signal outputted from the 2nd pulse delay means is carried out and a dummy pulse signal is generated and outputted, the number of insertion of a dummy pulse signal can be reduced. Thereby, without making power consumption increase not much, it is not concerned with a change in passage of an input pulse signal, but clock frequency change of a circuit can be made small, and a time delay can be stabilized.

[0020]

[Embodiment of the Invention]Hereafter, with reference to figures, an embodiment of the

invention is described in detail.

[A 1st embodiment] Drawing 1 and 2 are the figures showing the time delay stabilization circuit in a 1st embodiment that applied this invention.

[0021]First, composition is explained. Drawing 1 is a circuit diagram showing the time delay stabilization circuit 1 in a 1st embodiment, and the time delay stabilization circuit 1 comprises OR gate 50 which are the counter 100, the flip-flop 20, the dummy pulse generating circuit 30, and a pulse mixing circuit, the vernier 10, and the signal extracting circuit 40. The dummy pulse generating circuit 30 comprises the delay circuit 32, and the signal extracting circuit 40 comprises the flip-flop 41 and the delay circuits 42 and 43.

[0022]The cycle for the time delay of the request set up beforehand is calculated, and the counter 100 delays it from the count start signal which does not illustrate the inputted reference signal RCLK, and is outputted as signal TM1.

[0023]The flip-flop 20 makes data input signal TM1 inputted from the counter 100, and outputs signal TM2 which held signal TM1 by the rising edge to OR gate 50 by making into a clock pulse signal the reference signal RCLK which is the constant period T.

[0024]The delay circuit 32 is larger than the time delay of the flip-flop 20, and delays the inputted reference signal RCLK within the time of the cycle T and the difference of pulse width of the reference signal RCLK, and outputs delay clock signal DCLK to OR gate 50 as a dummy pulse signal.

[0025]OR gate 50 carries out OR operation of the delay clock signal DCLK inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and outputs it to the vernier 10 as mix-signals TD3.

[0026]The vernier 10 delays mix-signals TD3 inputted from OR gate 50 according to a preset value by the time resolution below the cycle T of the reference signal RCLK, and outputs it to the delay circuit 42 and the flip-flop 41 as delay pulse signal TD4.

[0027]The delay circuit 42 delay pulse signal TD4 inputted from the vernier 10, It is larger than the pulse width of the dummy pulse signal included in delay pulse signal TD4, and you make it delayed within the difference of the cycle T of the reference signal RCLK, and the time delay of the delay circuit 32, and it outputs to the flip-flop 41 as delay pulse signal TD5.

[0028]The flip-flop 41 makes data input delay pulse signal TD4 from the vernier 10, and outputs the signal TOUT which held delay pulse signal TD4 by the rising edge by making delay pulse signal TD5 from the delay circuit 42 into a clock pulse signal.

[0029]The delay circuit 43 delays the pulse width of the signal TOUT in time set up beforehand, and outputs the signal TOUT inputted from the flip-flop 41 as signal TM6. Signal TM6 outputted is inputted into the reset terminal of the flip-flop 41.

[0030]Drawing 2 is a timing chart which shows the state of each signal in the time delay stabilization circuit 1 of drawing 1. The signal delay of the circuit is omitted for simplification.

[0031]In drawing 2, the reference signal RCLK is a reference signal given to a circuit with the constant period T. Pulse width is the time T and signal TM1 is a signal which inputs arbitrary time with the resolution of the cycle T of the reference signal RCLK. Signal TM2 is the waveform which carried out 1 case shift of signal TM1 by the rising edge of the reference signal RCLK with the flip-flop 20. Delay clock signal DCLK is the waveform which delayed the reference signal RCLK T/4 by the delay circuit 32.
[0032]Mix-signals TD3 is the waveform which carried out OR operation of the delay clock signal DCLK to signal TM2 by OR gate 50. Since the pulse width of signal TM2 is wider than the pulse width of delay clock signal DCLK when signal TM2 and delay clock signal DCLK exist simultaneously, signal TM2 becomes the waveform which included delay clock signal DCLK.
[0033]Delay pulse signal TD4 is the waveform which delayed mix-signals TD3 Tx3/4 by the vernier 10 including fixed delay. Delay pulse signal TD5 is the waveform which delayed delay pulse signal TD4 Tx3/4 by the delay circuit 42.
[0034]The signal TOUT is the waveform which held delay pulse signal TD4 in the timing of the standup of delay pulse signal TD5 with the flip-flop 41. When the signal TOUT is the "Hi" level, the time delay of after flip-flop 41 of the delay circuit 43 is reset. Signal TM6 is the waveform which delayed the signal TOUT T/2 by the delay circuit 43.
[0035]Here, the example of a circuit of this invention of drawing 1 compares with the conventional circuit of drawing 6 the amount of change of the time delay of the output signal which considers the frequency change of an input signal as a reason.
[0036]In CMOS, following formula (1) - (3) is generally realized.
P=CxVxVxf -- (1)
Tj=Ta+thetaxP -- (2)
td=(A+BxTj) xtdta -- (3)
[0037]As for P, the load carrying capacity of a circuit and V the power consumption of a circuit, and C However, the power supply voltage of a circuit, As for the clock frequency of a circuit, and Ta, the temperature of a circuit and theta for f a room temperature and Tj The thermal resistance between a circuit and a room temperature, The time delay of a circuit [in / in tdta / a room temperature], the time delay of a circuit [in / in td / the temperature Tj], A, and B are a retardation coefficient without regards to temperature, and a retardation coefficient in connection with temperature, respectively, and A+BxTa=1 is realized.
[0038]First, the power consumption of a circuit is measured. In the following power consumption calculations, except the vernier 10 and a delay circuit, since circuit structure is small, it will not include in power consumption.
[0039]Since the frequency of signal TM2 inputted into the vernier 10 changes to 0 to a maximum of 1/(2xT), the power consumption of the example of the conventional circuit of

$$P=0 \sim C\times V\times V/(2\times T)$$
$$=0 \sim 1/2\times C\times V\times V/T$$

drawing 6 is from a formula (1).

It becomes ******.

[0040]Next, it asks for the power consumption of the example of a circuit of this invention of drawing 1. the vernier 10 and the delay circuits 32 and 42 -- each input signal TD3, RCLK, and TD4 is constant on 1/of frequency T, and the frequency of the input signal TOUT of the delay circuit 43 changes to 0-1/(2xT).

[0041]Here, if it is the same time delay, a delay circuit can be realized by the circuit structure of the half of a vernier, and it assumes that the load carrying capacity of circuit structure and a circuit is proportional, and asks for power consumption. As a standard, load carrying capacity in maximum delay = fixed delay + maximum variable delay =T/2+T=3/2xT of the vernier 10 is set to C.

[0042]Since each time delay of the delay circuits 32, 42, and 43 is T/4, Tx3/4, and T/2, load carrying capacity is set to C/12, Cx3/12, and C/6 based on assumption. Therefore, power consumption is xVxV/T+C/P=(C/12+C+Cx3/12) xVxV/T+C/6xVxVx0 - (C/12+C+Cx3/12) 6xVxV/(2xT) from a formula (1).

= It becomes the range of 4/3xCxVxV/T - 17/12xCxVxV/T.

[0043]The relation between amount of power variations deltaP and amount of delay change deltatd is delta td=Bxthetaxdelta Pxtdta from the difference of a formula (2) and a formula (3). -- (4)

It becomes.

[0044]The vernier 10 is concerned with timing accuracy in the example of the conventional circuit of drawing 6, and since the delaying amount is set to tdta=3/2xT, the amount of delay change serves as delta td=Bxtheta x(1/2xCxVxV/T-0) x3/2xT =0.75x BxthetaxCxVxV from a formula (4).

[0045]Since the vernier 10 and the delay circuit 42 are concerned with timing accuracy in the example of a circuit of this invention of drawing 1 and the delaying amount is set to tdta=3/2xT+3/4xT=9/4xT, the amount of delay change is from a formula (4).

$$\Delta td=B\times\theta\times(17/12\times C\times V\times V/T$$
$$-4/3\times C\times V\times V/T)\times 9/4\times T$$
$$\fallingdotseq 0.19\times B\times\theta\times C\times V\times V$$

It becomes.

[0046]If the case of the circuit of this invention of drawing 1 and the circuit which constituted the conventional system of drawing 6 from CMOS is compared, maximum electric power consumption is increasing by about 2.8 times, but the amount of power consumption change

decreases to one sixth, and the amount of delay change decreases to one fourth.

[0047][A 2nd embodiment] Drawing 3 and 4 are the figures showing the time delay stabilization circuit 3 in a 2nd embodiment that applied this invention. This time delay stabilization circuit 3 reduces power consumption by reducing the number of insertion of a dummy pulse compared with the time delay stabilization circuit 1 shown in drawing 1.

[0048]First, composition is explained. As shown in drawing 3, the time delay stabilization circuit 3, Comprise OR gate 50 which are the counter 100, the flip-flop 20, the dummy pulse generating circuit 30, and a pulse mixing circuit, and the dummy pulse generating circuit 30, Comprise OR gate 33, AND gate 35, delay circuit 32', and the flip-flop 34 and the dummy pulse equalizing circuit 300, and the dummy pulse equalizing circuit 300, It comprises AND gate 301, EXOR gate 302, the flip-flop 303, and NAND gate 304. It comes to be the composition same about the circuitry after OR gate 50 as the circuit shown in drawing 1 of a 1st embodiment of the above, and a graphic display and explanation are omitted about the composition.

[0049]In drawing 3, the counter 100 is outputted as signal TM1 which calculated the cycle for the time delay of the request set up beforehand, and delayed it from the count start signal which does not illustrate the inputted reference signal RCLK.

[0050]The flip-flop 20 makes signal TM1 data input, and outputs signal TM2 which held signal TM1 by the rising edge to OR gates 50 and 33 by making into a clock pulse signal the reference signal RCLK which is the constant period T.

[0051]OR gate 33 carries out OR operation of the inverted output signal MASK1B of signal TM2 and the flip-flop 34 which were inputted from the flip-flop 20, and outputs signal MASK1 to the flip-flop 34.

[0052]The flip-flop 34 makes data input signal MASK1 inputted from OR gate 33, and makes the reference signal RCLK a clock pulse signal, Inverted output signal MASK1B which held the logic inversion of signal MASK1 by the rising edge is outputted to OR gate 33, AND gate 35, and AND gate 301.

[0053]Delay circuit 32' outputs delay clock signal DCLK which exceeded the sum total of the time delay of the flip-flop 303 and NAND gate 304 for the inputted reference signal RCLK, and delayed the time within the cycle T and the difference of pulse width of the reference signal RCLK to AND gate 35.

[0054]Signal MASK1B into which AND gate 35 was inputted from the flip-flop 34, The dummy pulse signal HCLK which carried out the AND operation of the delay clock signal DCLK inputted as signal MASK2B inputted from the dummy pulse equalizing circuit 300 from delay circuit 32' is outputted to OR gate 50.

[0055]OR gate 50 outputs mix-signals TD3 which carried out OR operation of the dummy pulse signal HCLK to signal TM2. About the circuitry after mix-signals TD3, since it becomes circuitry

shown in drawing 1, and the same composition, a graphic display and explanation are omitted.

[0056]The composition of the dummy pulse equalizing circuit 300 is explained below. AND gate 301 outputs the signal TOGL which carried out the AND operation of signal TM1 and the signal MASK1B inputted from the flip-flop 34 to EXOR gate 302.
[0057]EXOR gate 302 outputs signal MASK20 which did the exclusive theoretical sum operation of the signal MASK21 inputted from the signal TOGL inputted from AND gate 301, and the flip-flop 303 to the flip-flop 303.
[0058]The flip-flop 303 makes data input signal MASK20 inputted from EXOR gate 302, Signal MASK21 which held signal MASK20 by the rising edge by making the reference signal RCLK into a clock pulse signal is outputted to EXOR gate 302 and NAND gate 304.
[0059]NAND gate 304 outputs signal MASK2B which carried out the AND operation of signal TM1 and the signal MASK21 which were inputted from the flip-flop 303, and was reversed to AND gate 35.
[0060]Drawing 4 is a timing chart which shows the state of each signal in the time delay stabilization circuit 3 of drawing 3. The signal delay of the circuit is omitted for simplification.
[0061]In drawing 4, the reference signal RCLK is a reference signal given to a circuit with the constant period T. Pulse width is the time T and signal TM1 is a signal which inputs arbitrary time with the resolution of the cycle T of the reference signal RCLK. Signal TM2 is the waveform which carried out 1 case shift of signal TM1 by the rising edge of the reference signal RCLK with the flip-flop 20.
[0062]Delay clock signal DCLK is the waveform which delayed the reference signal RCLK T/4 by delay circuit 32'. Signal MASK1 is the waveform which carried out OR operation of the signal MASK1B to signal TM2 by OR gate 33.
[0063]Signal MASK1B is the waveform which carried out 1 case shift of signal MASK1 by the rising edge of the reference signal RCLK, and also carried out logic inversion with the flip-flop 34. That is, it is the timing of the rising edge of the reference signal RCLK, the inverted output of the flip-flop 34 will be initialized on the "Lo" level, if signal TM2 is the "Hi" level, and if signal TM2 is the "Lo" level, it will repeat a level and "Hi" "Lo" level by turns.
[0064]The signal TOGL is the waveform which carried out the AND operation of the signal TM1 and signal MASK1B by AND gate 301. Signal MASK20 is the waveform which carried out EXCLUSIVE OR operation of signal MASK21 to the signal TOGL by EXOR gate 302. Signal MASK21 is the waveform which carried out 1 case shift of signal MASK20 in the timing of the standup of the reference signal RCLK with the flip-flop 303.
[0065]Signal MASK2B is the waveform which carried out the AND operation of signal MASK21 and signal TM1, and carried out logic inversion by NAND gate 304. The dummy pulse HCLK is the waveform which carried out the AND operation of the delay clock signal DCLK ** to signal

MASK1B and MASK2B by AND gate 35.

[0066]Therefore, the dummy pulse signal HCLK is not outputted by signal MASK1B with the cycle of the following reference signal RCLK, when signal TM2 is the "Hi" level, but when signal TM2 is the "Lo" level, it is outputted once to two cycles of the reference signal RCLK.

[0067]When signal TM1 is inputted by signal MASK2B for every odd number cycle of the reference signal RCLK, the dummy pulse signal HCLK prevents insertion of the dummy pulse signal inserted once just before signal TM2 to the 2 times, and equalizes clock frequency by it.

[0068]Mix-signals TD3 is the waveform which carried out OR operation of the dummy pulse signal HCLK to signal TM2 by OR gate 50, Since the pulse width of signal TM2 is wider than the width of the dummy pulse signal HCLK when signal TM2 and the dummy pulse signal HCLK exist simultaneously, signal TM2 becomes the waveform which included the dummy pulse signal HCLK.

[0069]Except that the numbers of dummy pulse signal insertion differ, since the circuitry of the waveform after TD3 is the same as that of drawing 2, it omits explanation.

[0070]Next, operation of the dummy pulse equalizing circuit 300 is explained. If the cycle of the reference signal RCLK is inputted and signal TM1 is inputted into AND gate 301 every odd pieces, the output signal TOGL of AND gate 301 will serve as the "Hi" level. By and EXOR gate 302 into which the signal TOGL was inputted from AND gate 301. Since the data input of the signal MASK20 which carried out logic inversion of output signal MASK21 of the flip-flop 303 is carried out to flip-flop 303 self, whenever the above-mentioned conditions are satisfied, signal MASK21 repeats "Hi" "Lo" level by turns with a level.

[0071]Before 1 cycle from which signal TM2 is set to the "Hi" level, NAND gate 304 prevents insertion of a dummy pulse signal by AND gate 35 by using MASK2B as the "Lo" level, when signal TM1 is the "Hi" level, and signal MASK21 is the "Hi" level.

[0072]On the other hand, NAND gate 304 inserts a dummy pulse signal by AND gate 35, when signal TM1 does not input, or when signal MASK21 is the "Lo" level. Therefore, even if signal TM1 is inputted for every odd number cycle of the reference signal RCLK, the dummy pulse signal inserted just before signal TM2 is prevented once by the 2 times, and the frequency of an average of signal TD3 is not concerned with the input frequency of signal TM1, but is equalized to 1/(2xT).

[0073]Next, it asks for the power consumption of the example of a circuit of this invention of drawing 3. The input signal RCLK of delay circuit 32' is constant on 1/of frequency T, the frequency of an average of input signal TD3 of the vernier 10 and the delay circuit 42 and TD4 is constant at 1/(2xT), and the frequency of the input signal TOUT of the delay circuit 43 changes to 0-1/(2xT). Since each time delay of the delay circuits 32, 42, and 43 is T/4, Tx3/4, and T/2, load carrying capacity is set to C/12, Cx3/12, and C/6 based on assumption. Therefore, power consumption is P=C/12xVxV/T+(C+Cx3/12) xVxV/(2xT) from a formula (1).

+ C/6xVxVx0 - C/12xVxV/T+(C+Cx3/12) xVxV/(2xT)
+ C/6xVxV/(2xT)
= It becomes the range of 17/24xCxVxV/T - 19/24xCxVxV/T.

[0074]Next, the amount of delay change is calculated. Since it is the vernier 10 and the delay circuit 42 that the amount of delay change in the example of a circuit of this invention of drawing 4 is concerned with timing accuracy and the delaying amount is set to tdta=3/2xT+3/4xT=9/4xT, The amount of delay change serves as delta td=Bxtheta x (19/24xCxVxV/T-17/24xCxVxV/T) x9/4xT =0.19x BxthetaxCxVxV from a formula (4).

[0075]If the case where this invention of drawing 3 and the conventional system of drawing 6 are constituted from CMOS is compared, maximum electric power consumption is increasing by about 1.6 times, but the amount of power consumption change decreases to one sixth, and the amount of delay change decreases to one fourth.

[0076]The above result is summarized and the graph of the amount of delay change and power consumption is shown in drawing 5. It is the graph with which the graph of drawing 5 (b) showed the power consumption for the amount of delay change of the output signal TOUT when the graph of drawing 5 (a) changes the frequency of input signal TM1 to 0-1/(2xT), and the relative comparison of the two examples of a circuit of this invention was carried out on the basis of the case where a circuit is conventionally constituted from CMOS.

[0077]Although each of two examples of a circuit of this invention has power consumption conventionally larger than the example of a circuit, since the amount of change of power consumption can be made small, it is more possible than the graph of drawing 5 to make the amount of delay change conventionally smaller than the example of a circuit.

[0078]Usually, in IC, two or more such detailed timing generating circuits are carried. For example, when 20 detailed timing generating circuits are carried, the amount of change of the power consumption in the worst conditions is expanded by 20 times, and, therefore, the amount of delay change is also expanded by 20 times. Supposing there is delay change of 50ps now in one detailed timing generating circuit, the amount of change will be expanded to a maximum of 20 times as many 1000ps.

[0079]On the other hand, this effect is size, when the amount of delay change can be reduced to one fourth of about 250 ps and it sees as an LSI tester by applying this invention to a detailed timing generating circuit.

[0080]Although positive logic explained all the examples, they can also consist of negative logic. Although the fixed value explained the delaying amount of the vernier and the delay circuit, it can also be changed in the range in which the circuit operates. Although CMOS explained the circuit, since it is the character of a semiconductor to change a time delay with temperature not a little, this circuit system is applicable also to circuits other than CMOS.

[0081]

[Effect of the Invention]According to the time delay stabilization circuit of the invention according to claim 1, it is not concerned with the change in passage of a view signal, but clock frequency change of the vernier 10 can be made small. Since power consumption change of the vernier 10 becomes small by this, a temperature change becomes small and can stabilize a time delay.

[0082]According to the time delay stabilization circuit of the invention according to claim 2, the dummy pulse from which pulse width differs can be inserted between the view signal and view signal which are inputted into a vernier and which you want to delay, and clock frequency change of a circuit can be made small.

[0083]Since according to the time delay stabilization circuit of the invention according to claim 3 a view signal and a dummy pulse are distinguished by the difference in pulse width and only a view signal can be extracted, a circuit and the time delay stabilization circuit which performs same operation can be constituted conventionally.

[0084]According to the time delay stabilization circuit of the invention according to claim 4, the number of insertion of a dummy pulse signal can be reduced. Thereby, without making power consumption increase greatly, it is not concerned with the change in passage of a view signal, but clock frequency change of a circuit can be made small, and a time delay can be stabilized.

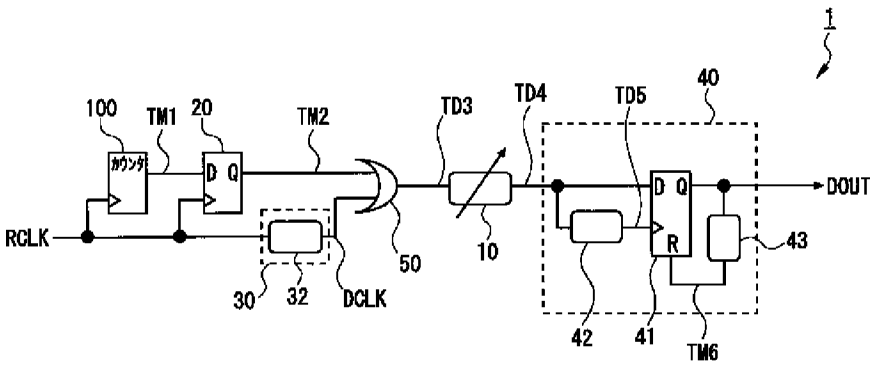
[Translation done.]

* NOTICES *

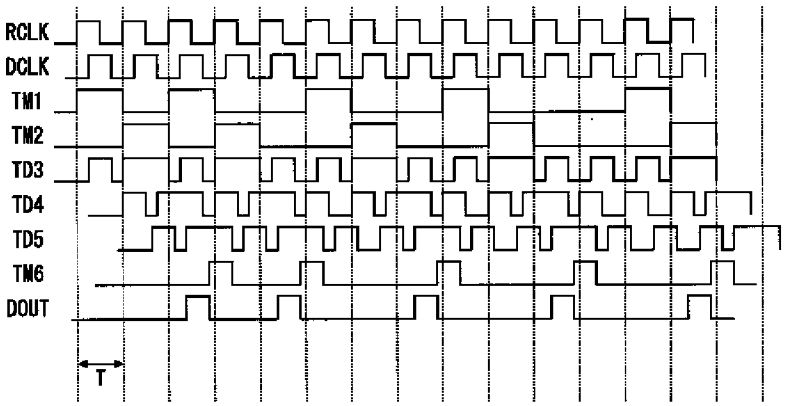
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

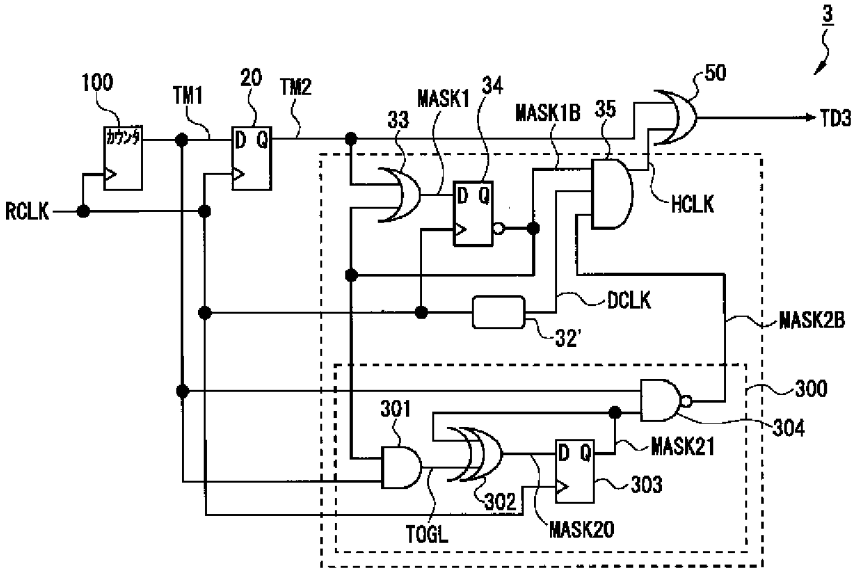
[Drawing 1]



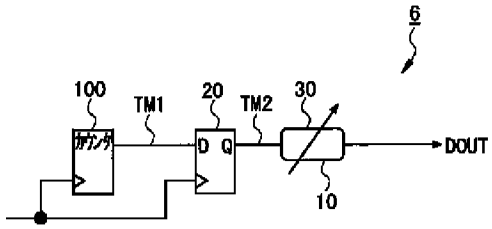
[Drawing 2]



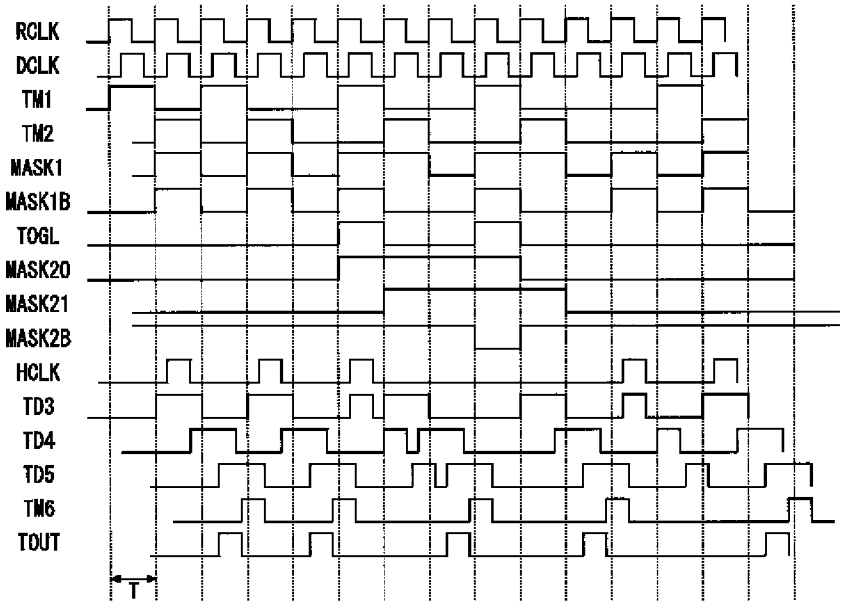
[Drawing 3]



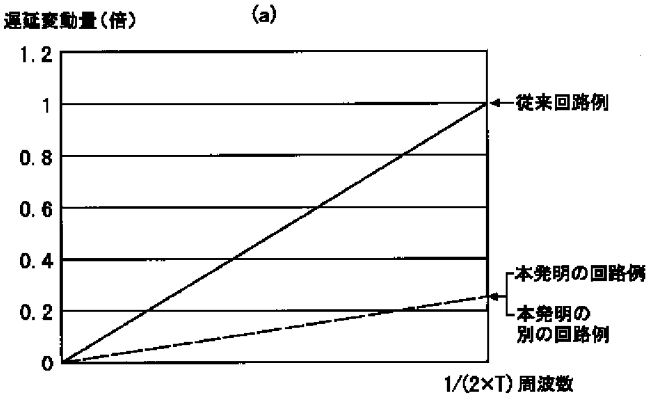
[Drawing 6]

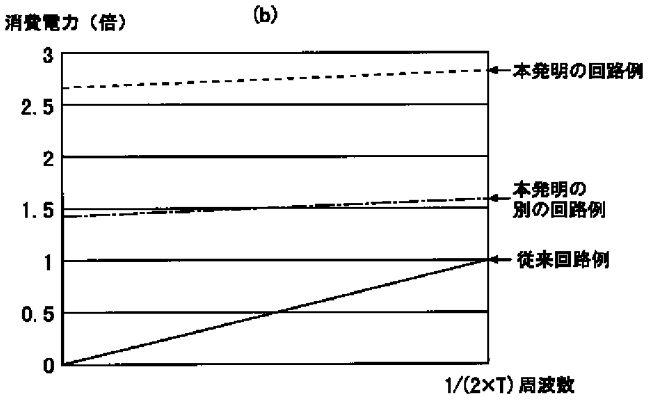


[Drawing 4]

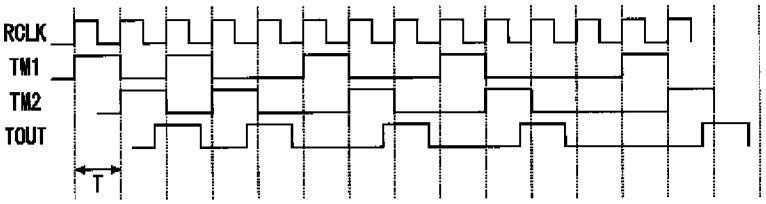


[Drawing 5]





[Drawing 7]



[Translation done.]